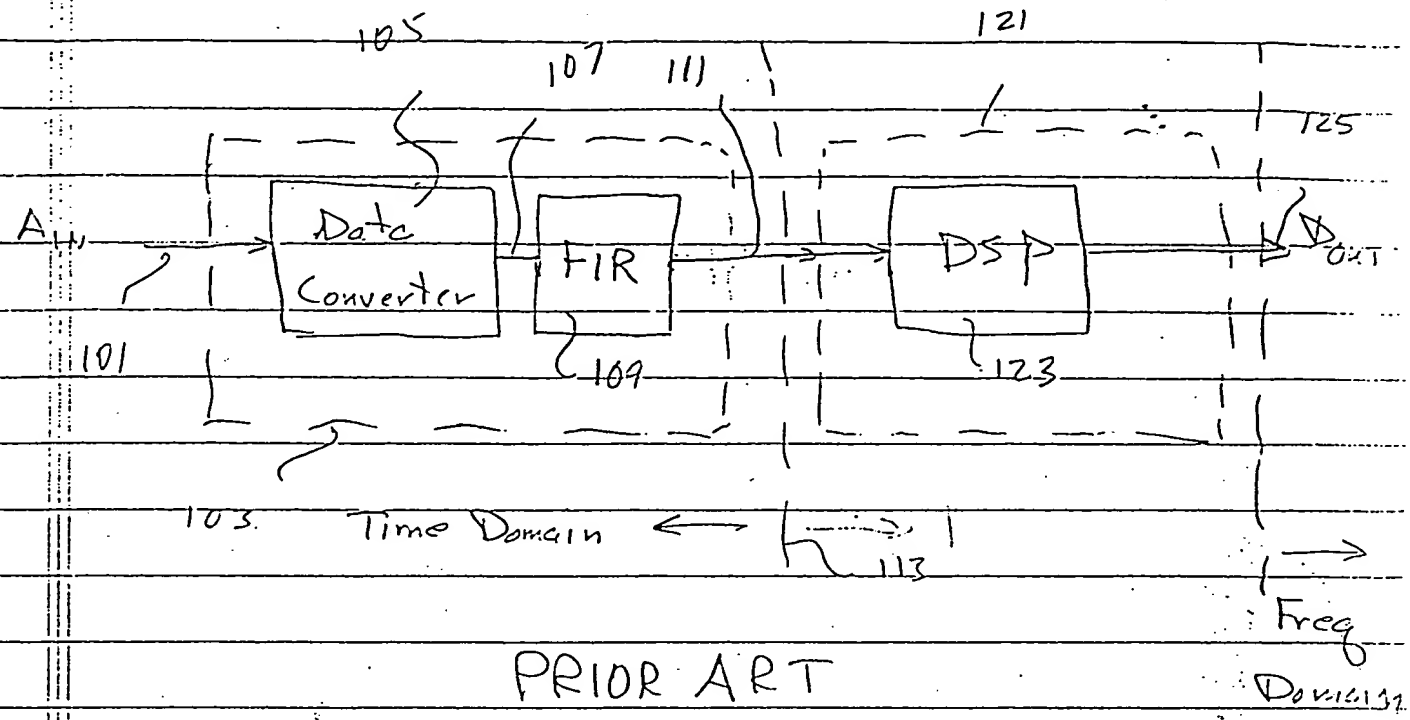

PRIOR ART

FIG 1

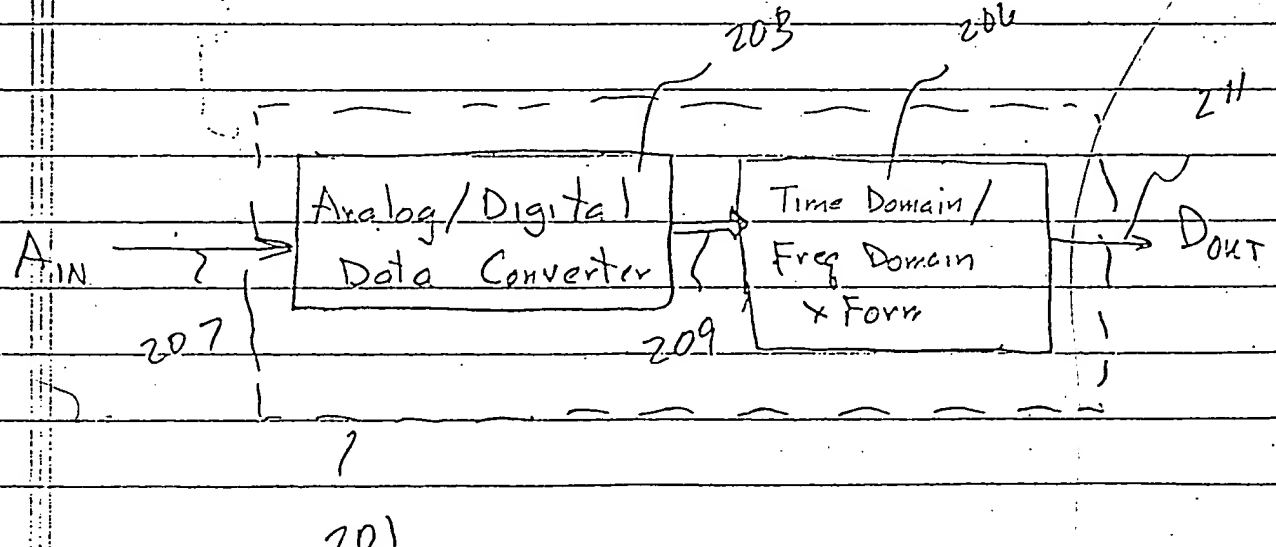

FIG 2

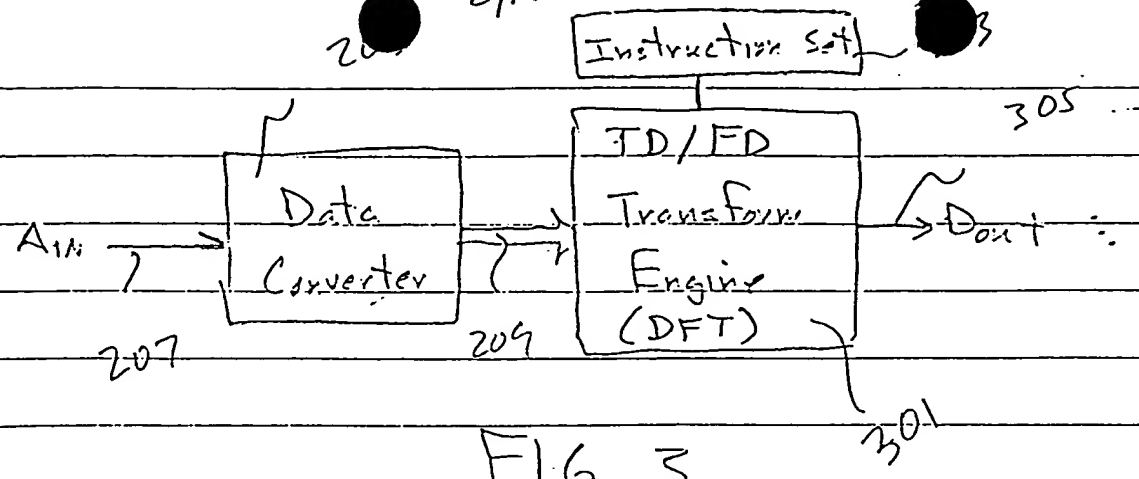
Instruction Set
TD/FD Transform Engine (DFT)
305
Data Converter
A_{IN}
D_{OUT}
207
209
301

FIG 3

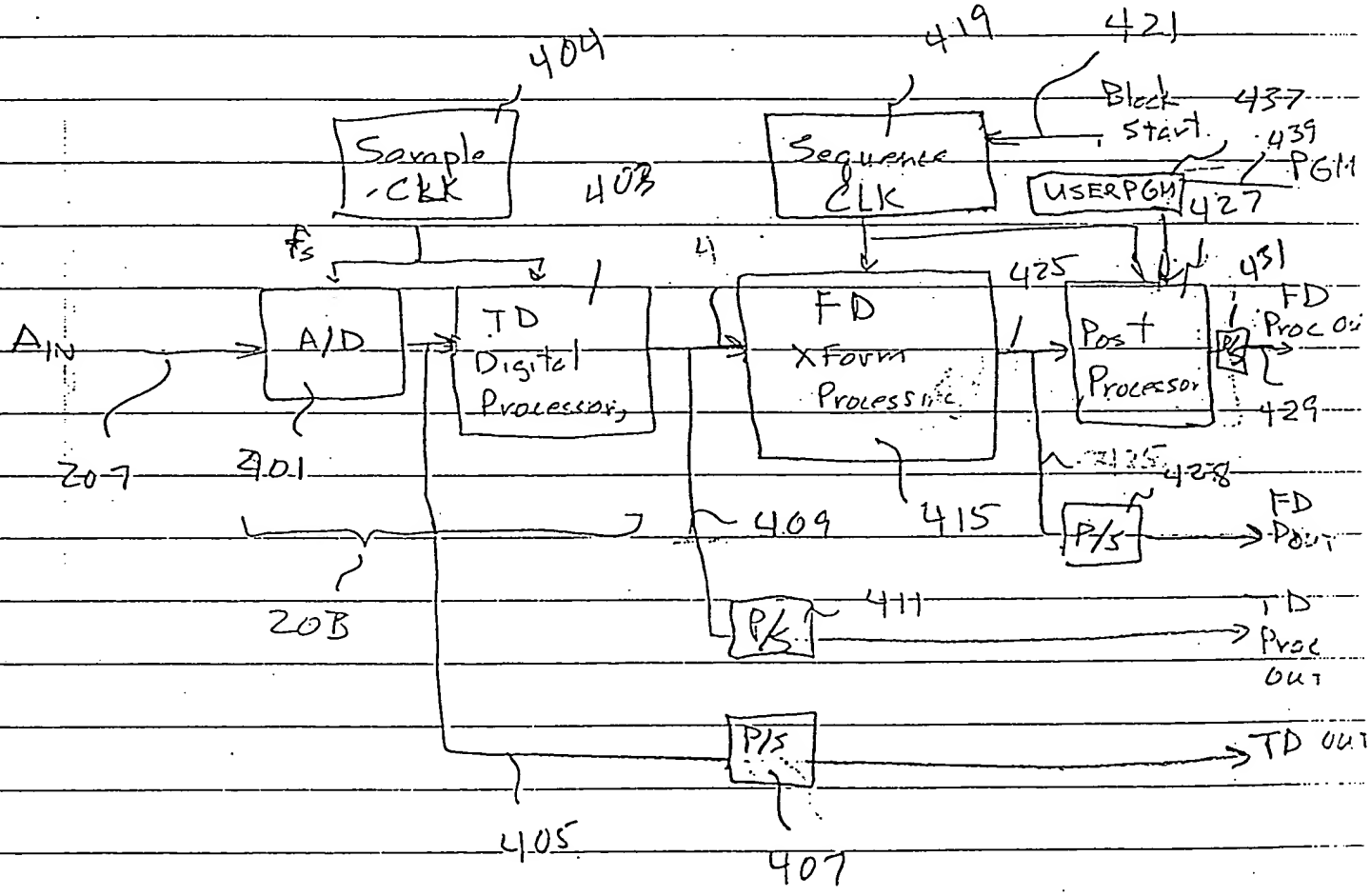
404
419
421
Sample Clk
Sequence CLK
Block Start
437
439
PGM
USERPGM
427
408
f_s
4
425
451
A_{IN}
A/D
TD Digital Processor
FD XForm Processing
Post Processor
FD Proc Out
429
207
401
428
409
415
FD Pout
P/S
411
TD Proc Out
TD Out
405
407

FIG 4

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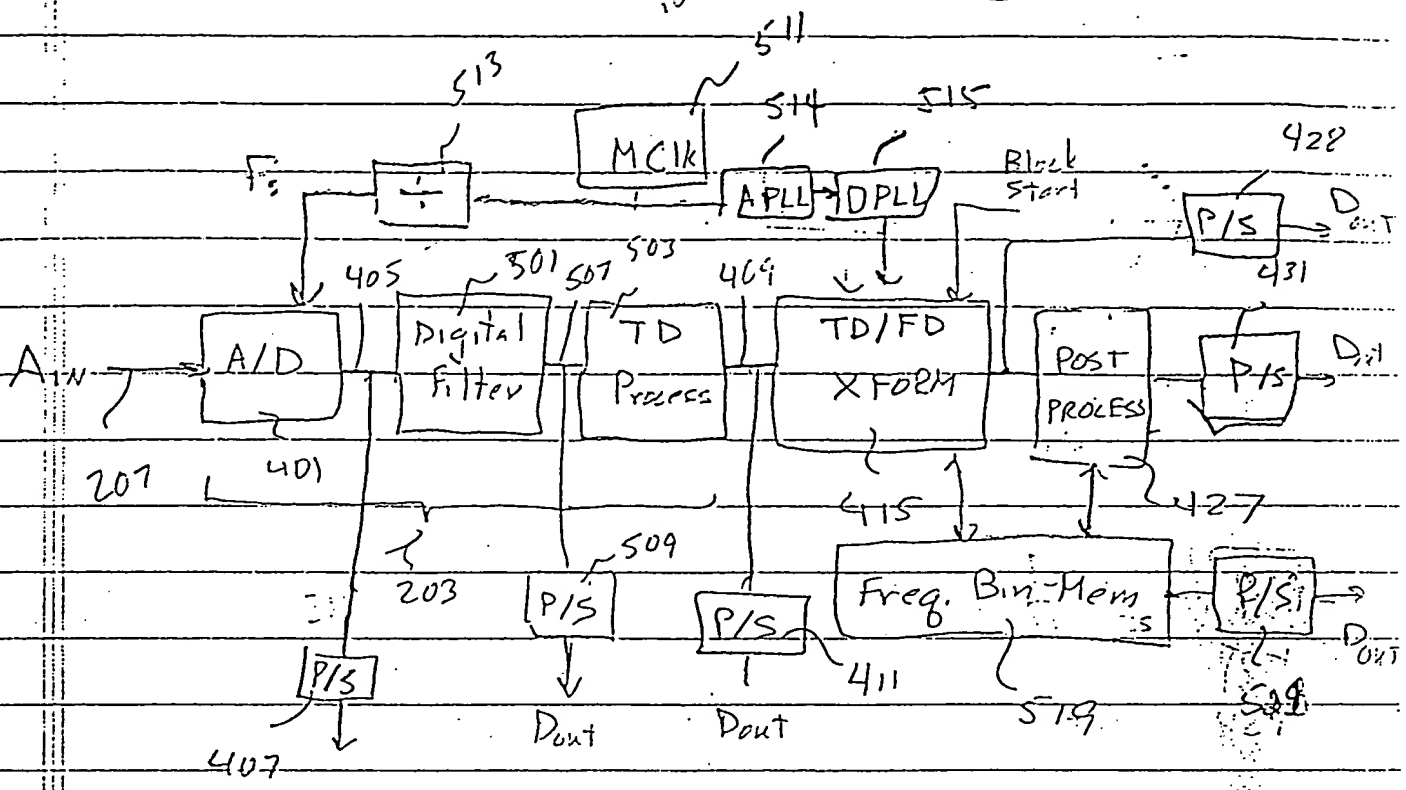

FIG 5

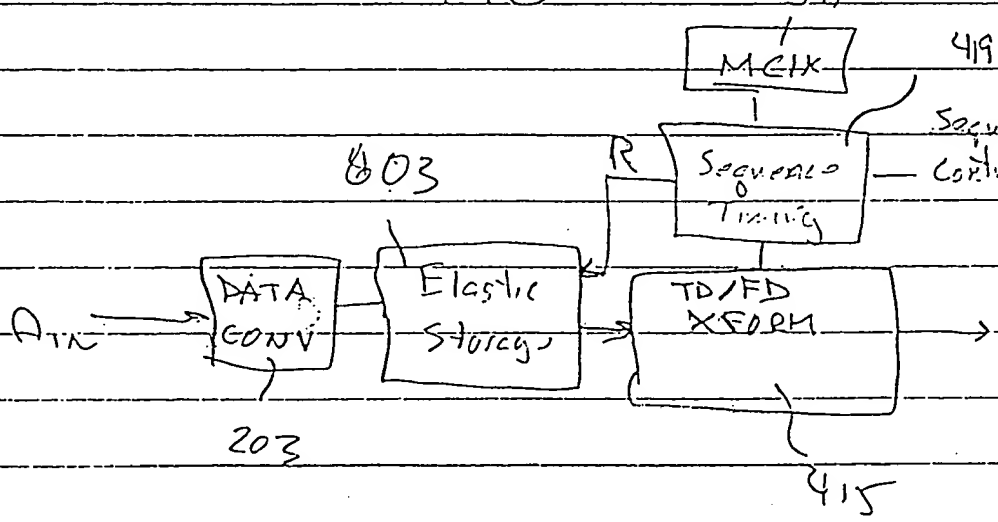

FIG 6

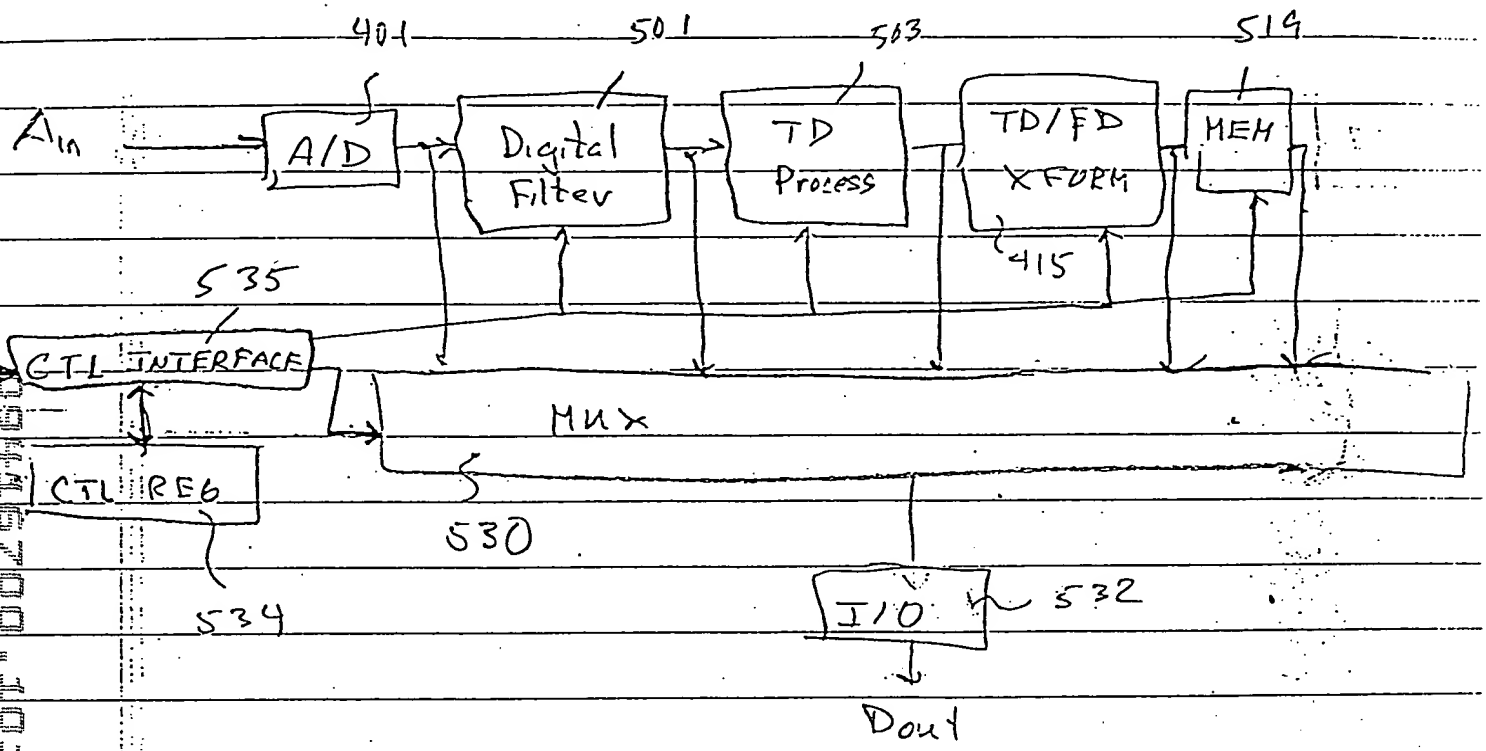
401
501
503
519
Ain
A/D
Digital Filter
TD Process
TD/FD XFORM
MEM
415
535
GTL INTERFACE
MUX
CTL REG
530
534
I/O
532
Dout

FIG 5a

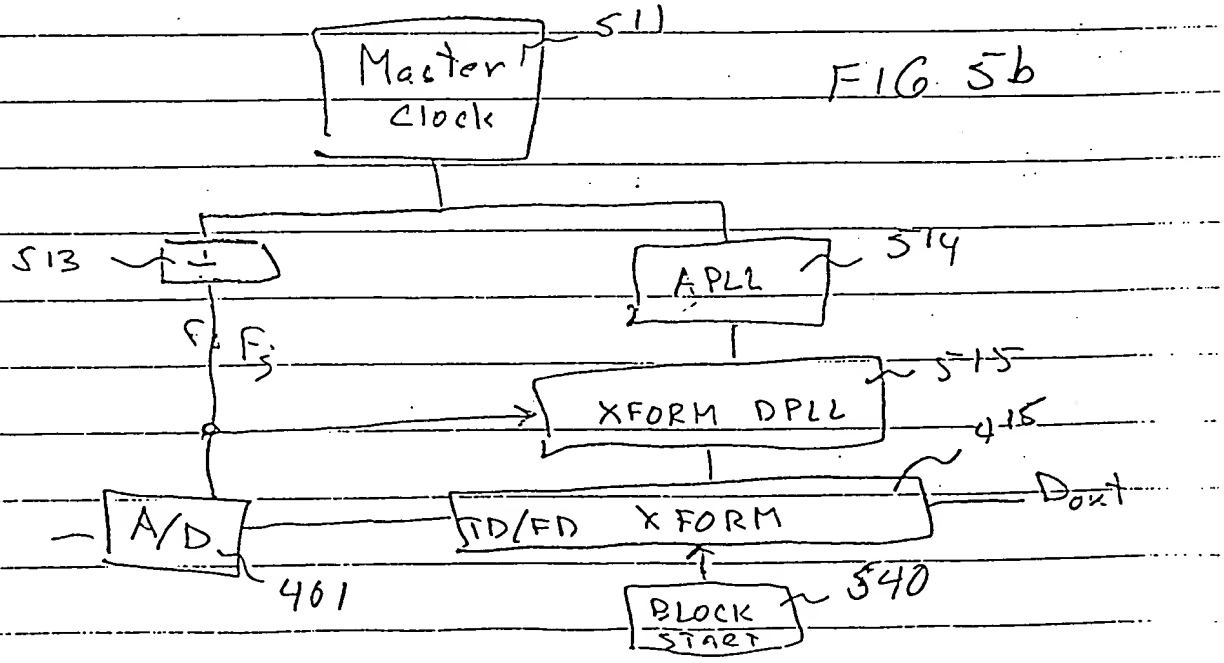
Master Clock
511
513
÷
APLL
514
Fs
XFORM DPLL
515
416
A/D
TD/FD XFORM
Dout
401
BLOCK START
540

FIG 5b

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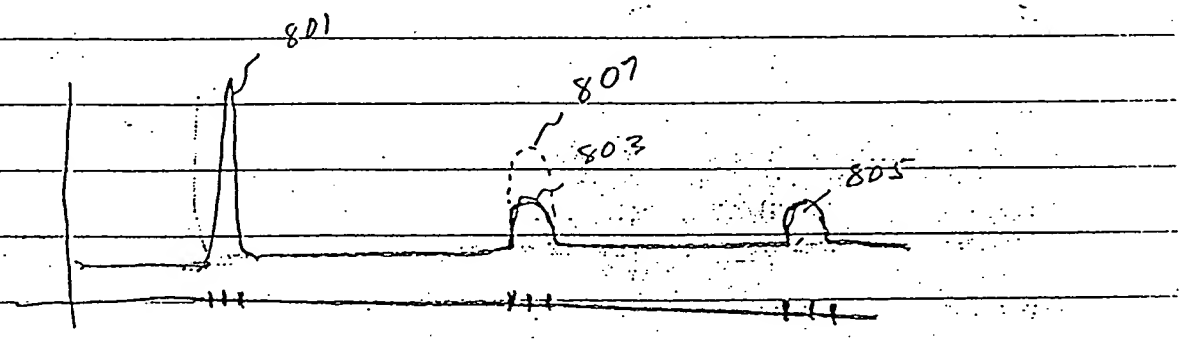

FIG 7

0622.0057750

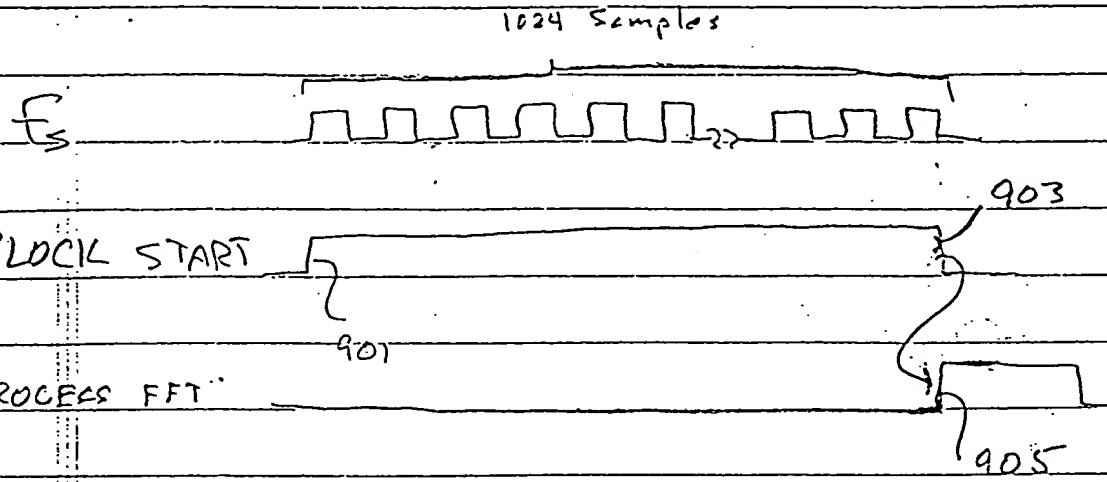
1024 Samples
f_s
903
BLOCK START
901
PROCESS FFT
905

FIG 8

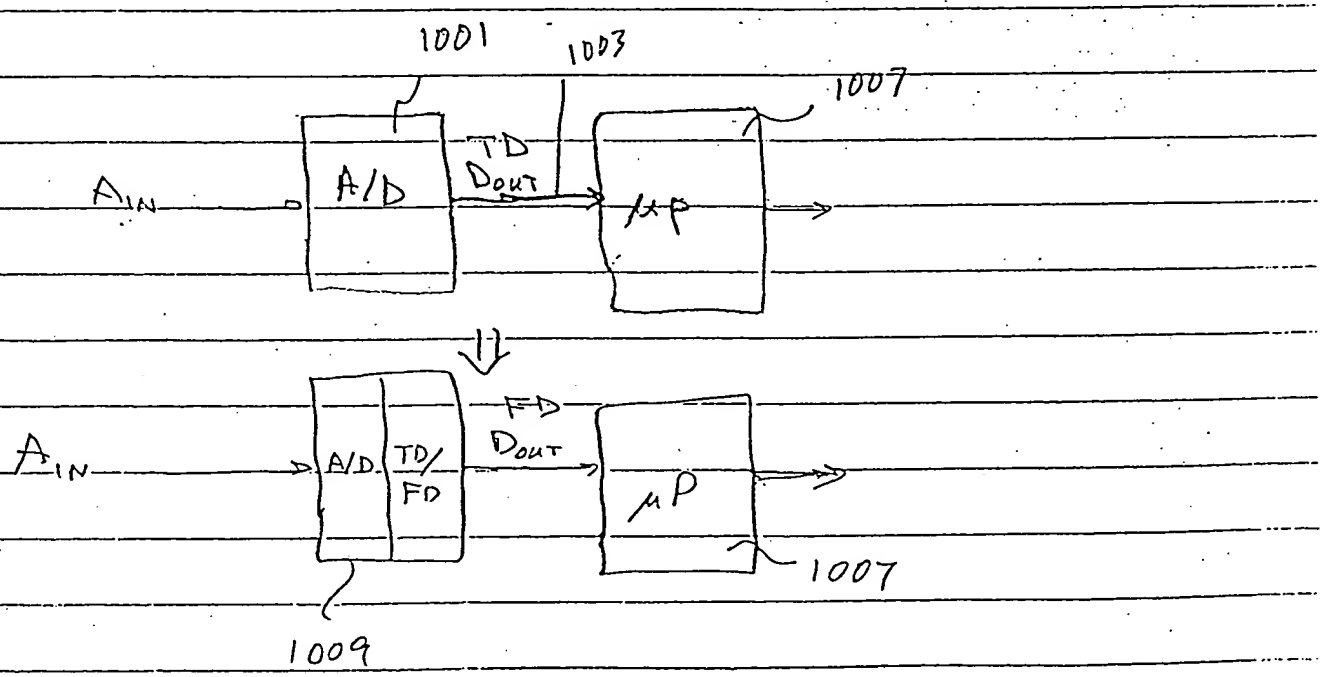
1001
1003
1007
A_{IN}
A/D
TD
D_{OUT}
µP
A_{IN}
A/D
TD/
FD
FD
D_{OUT}
µP
1007
1009

FIG 9

HC[redacted] 24,805
7/24

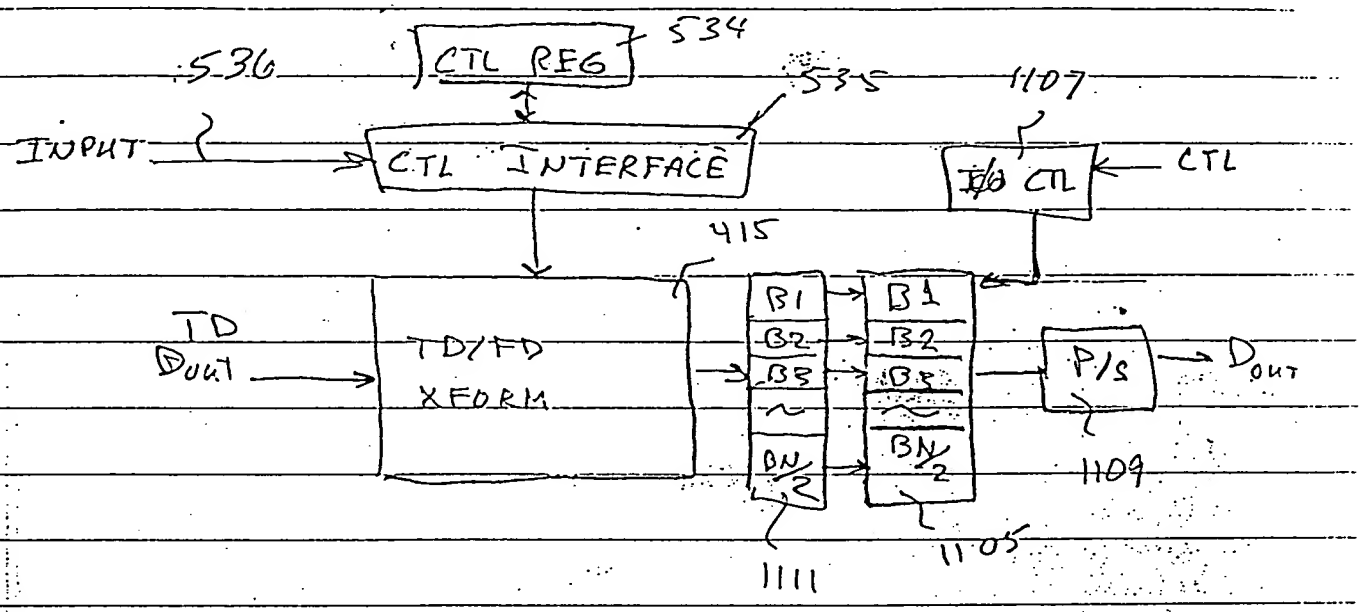

FIG 10

0052700.0052700

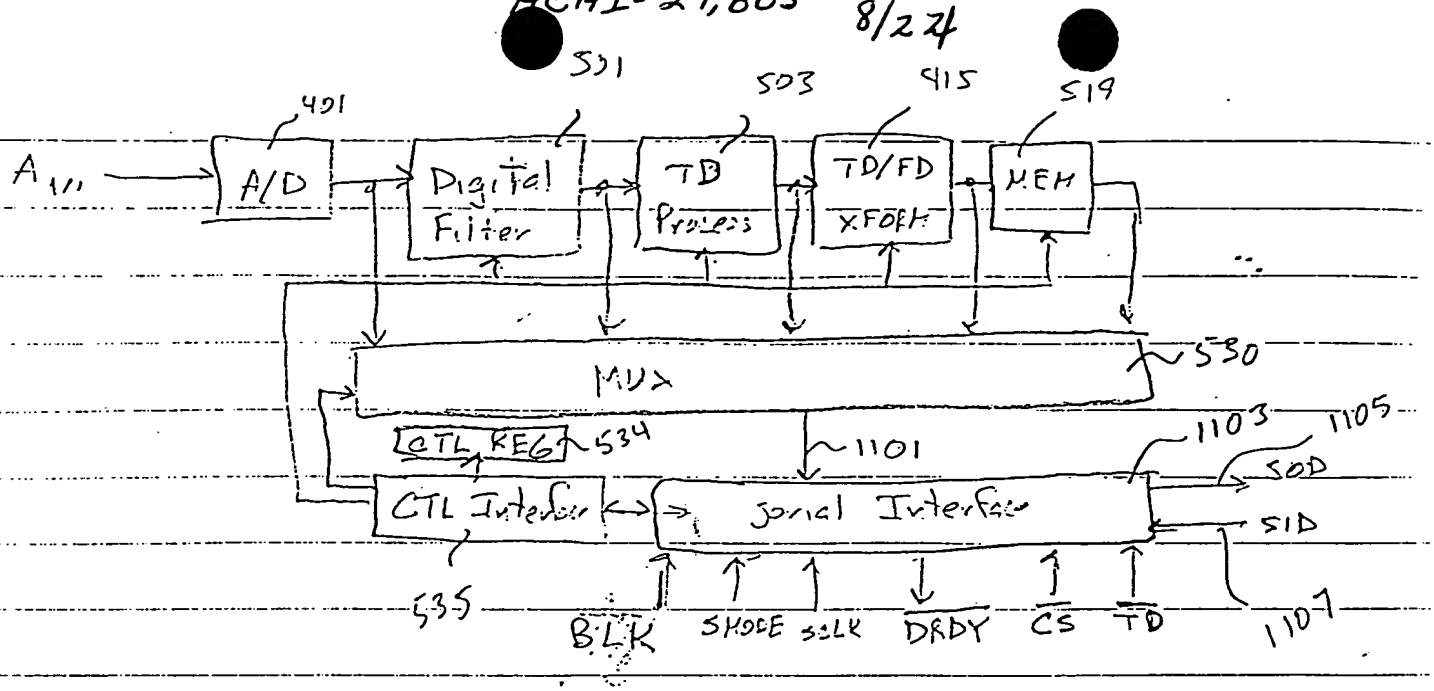

FIG 11

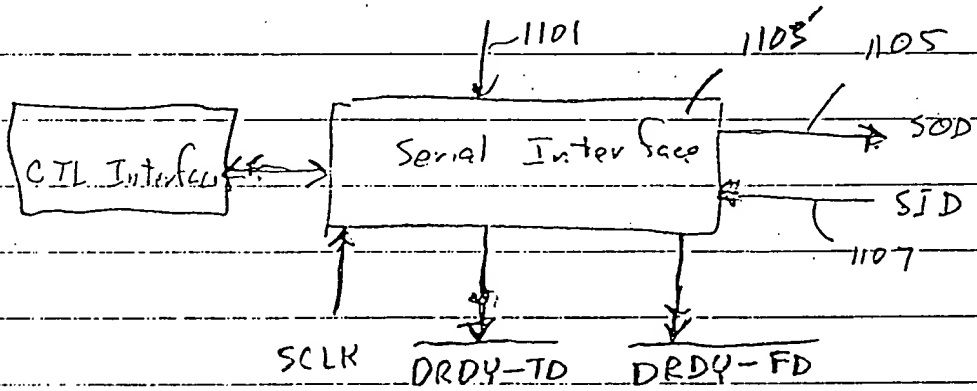

FIG 11a

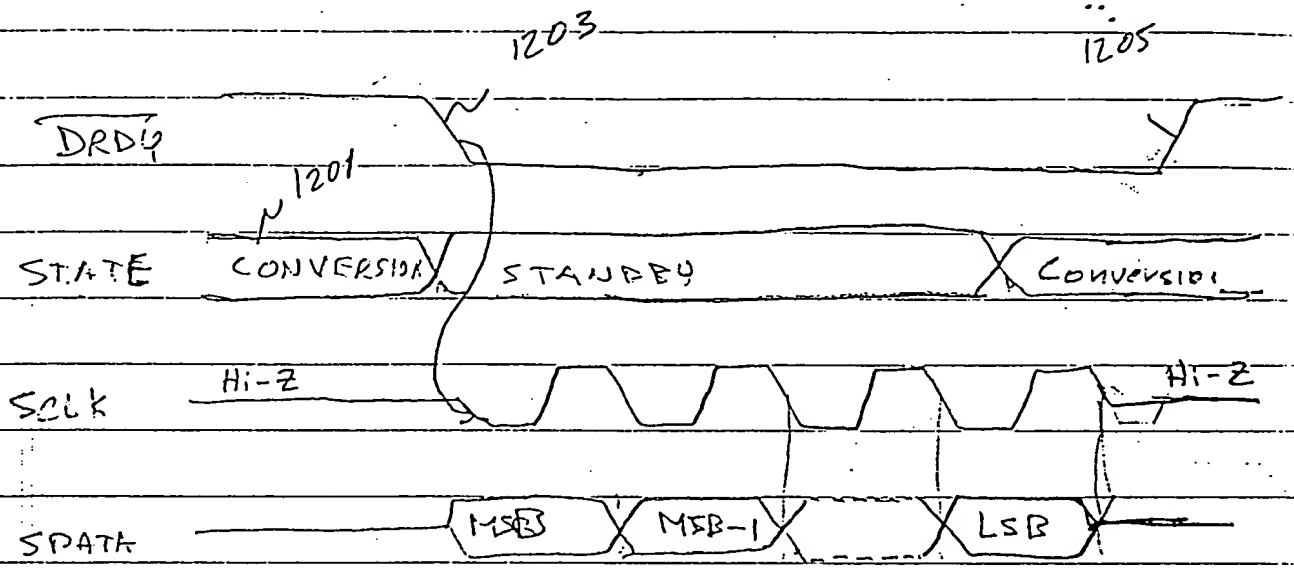

FIG 12

Document ID: 4004

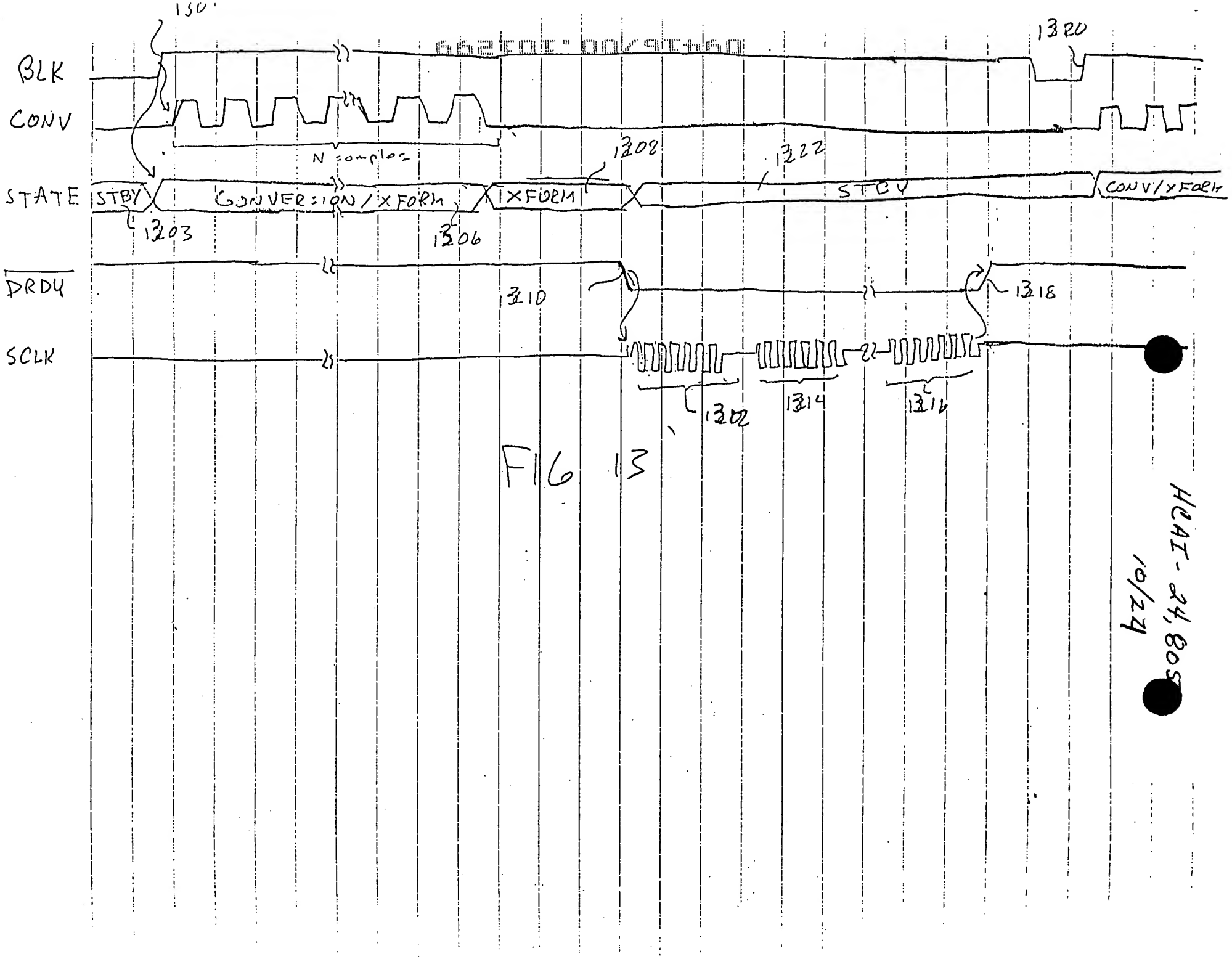

FIG 13

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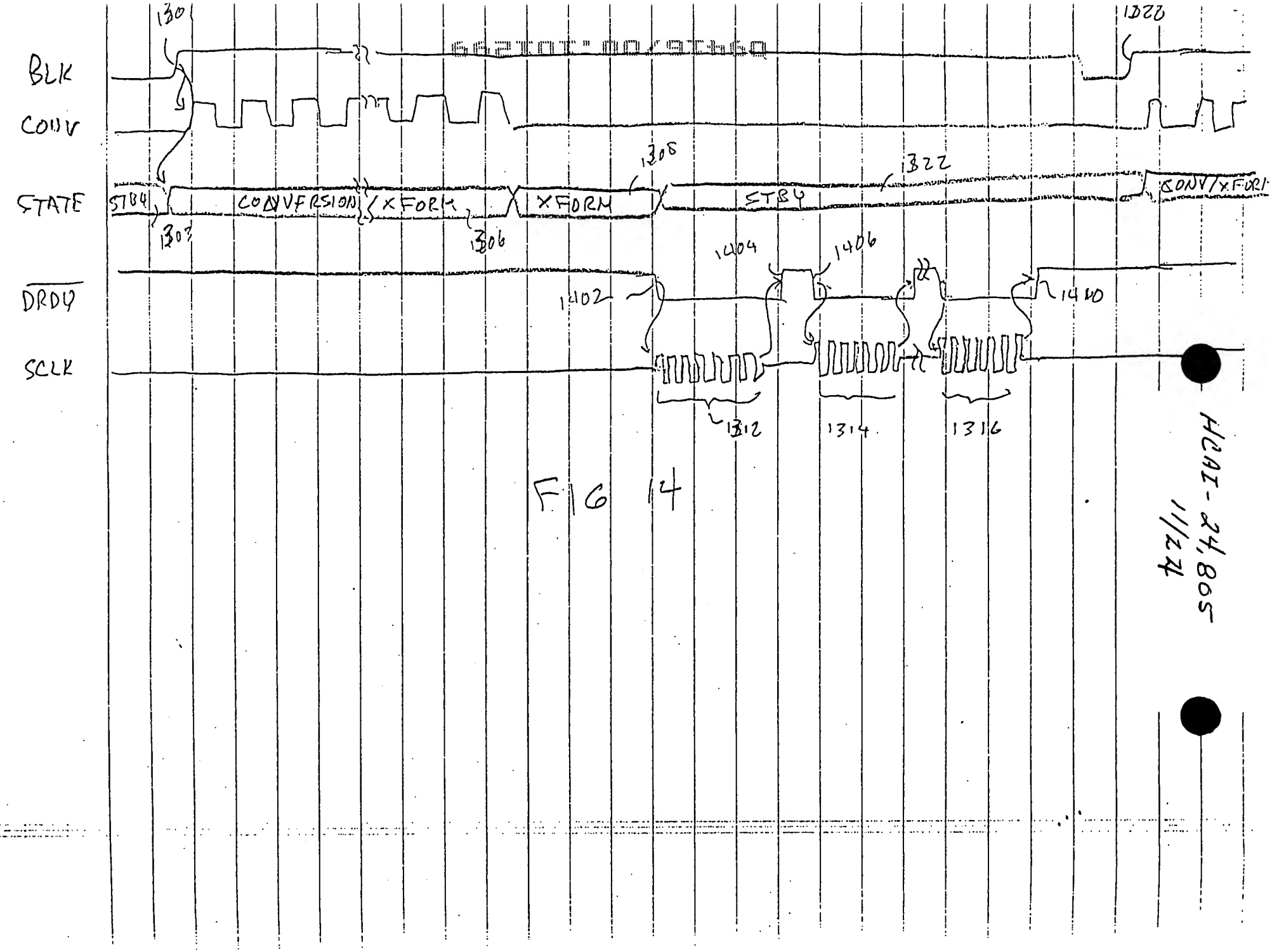

FIG 14

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HCAI-[illegible],805
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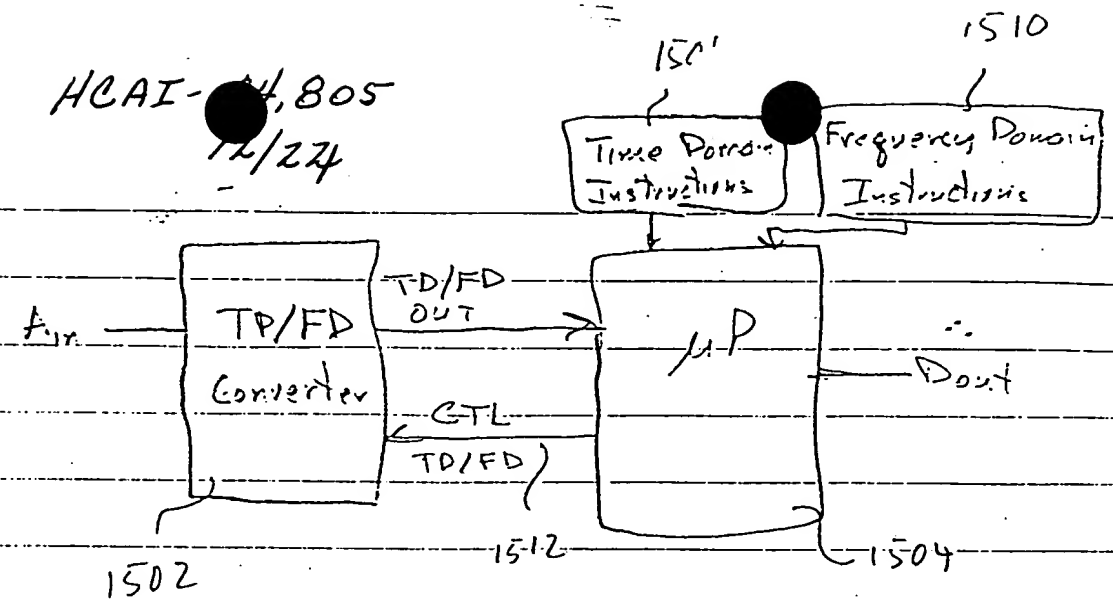


FIG 15

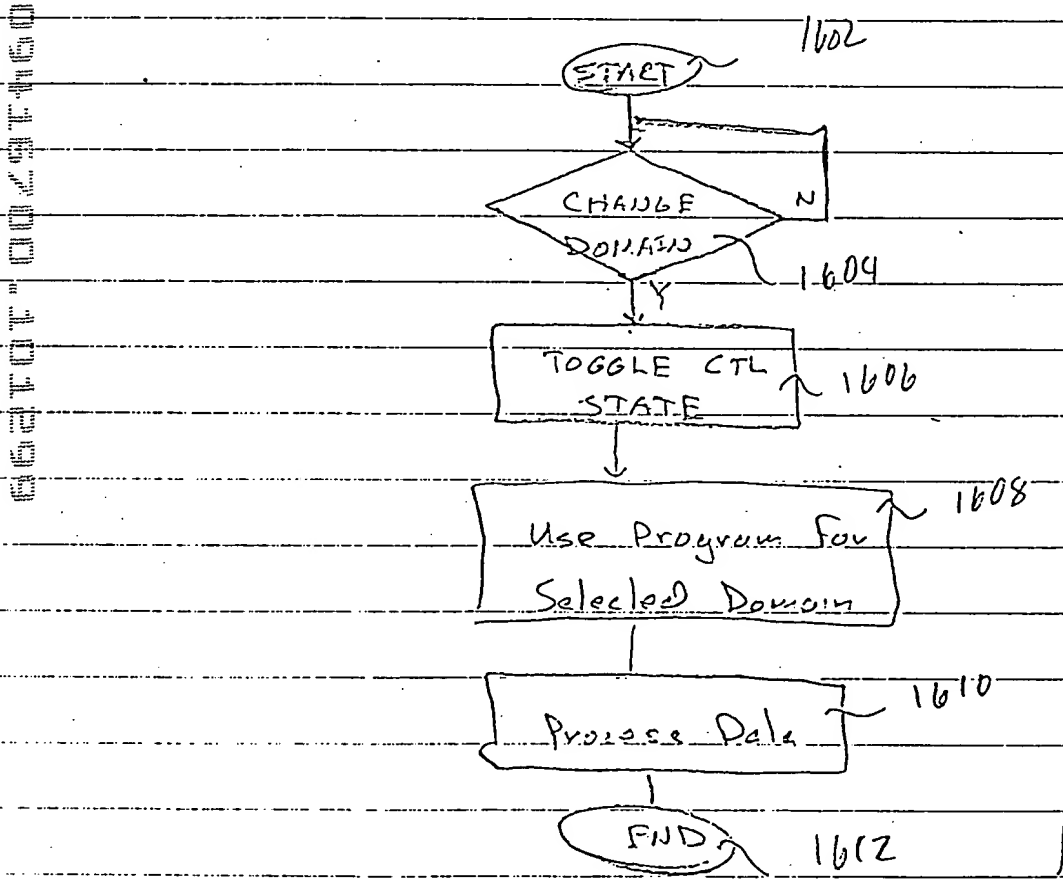
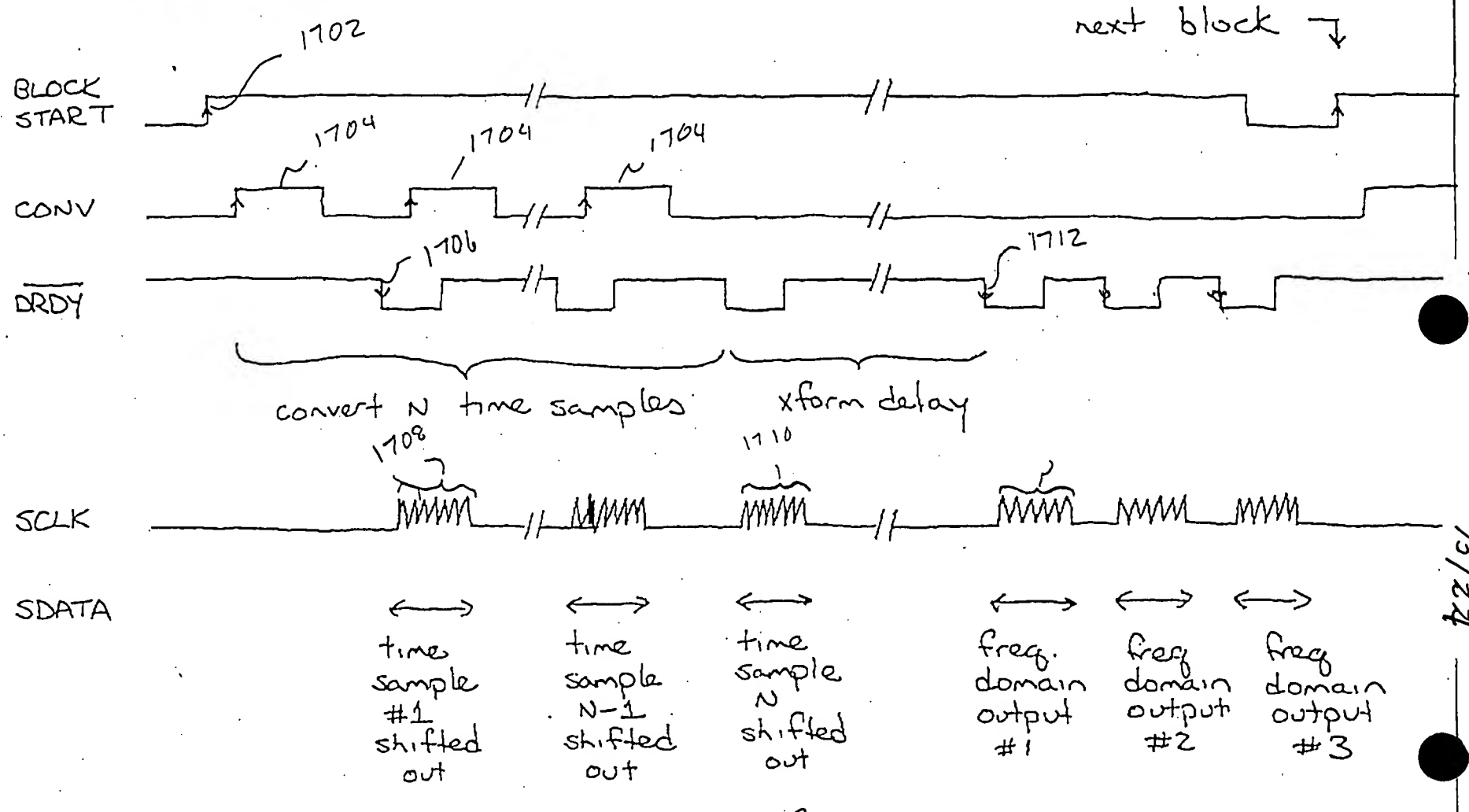


FIG 16

662TOT*0079Th60

Hybrid $\overline{\text{DRDY}}$ Mode



F16 17

H/HAI-24,805 13/24

HI-24,805
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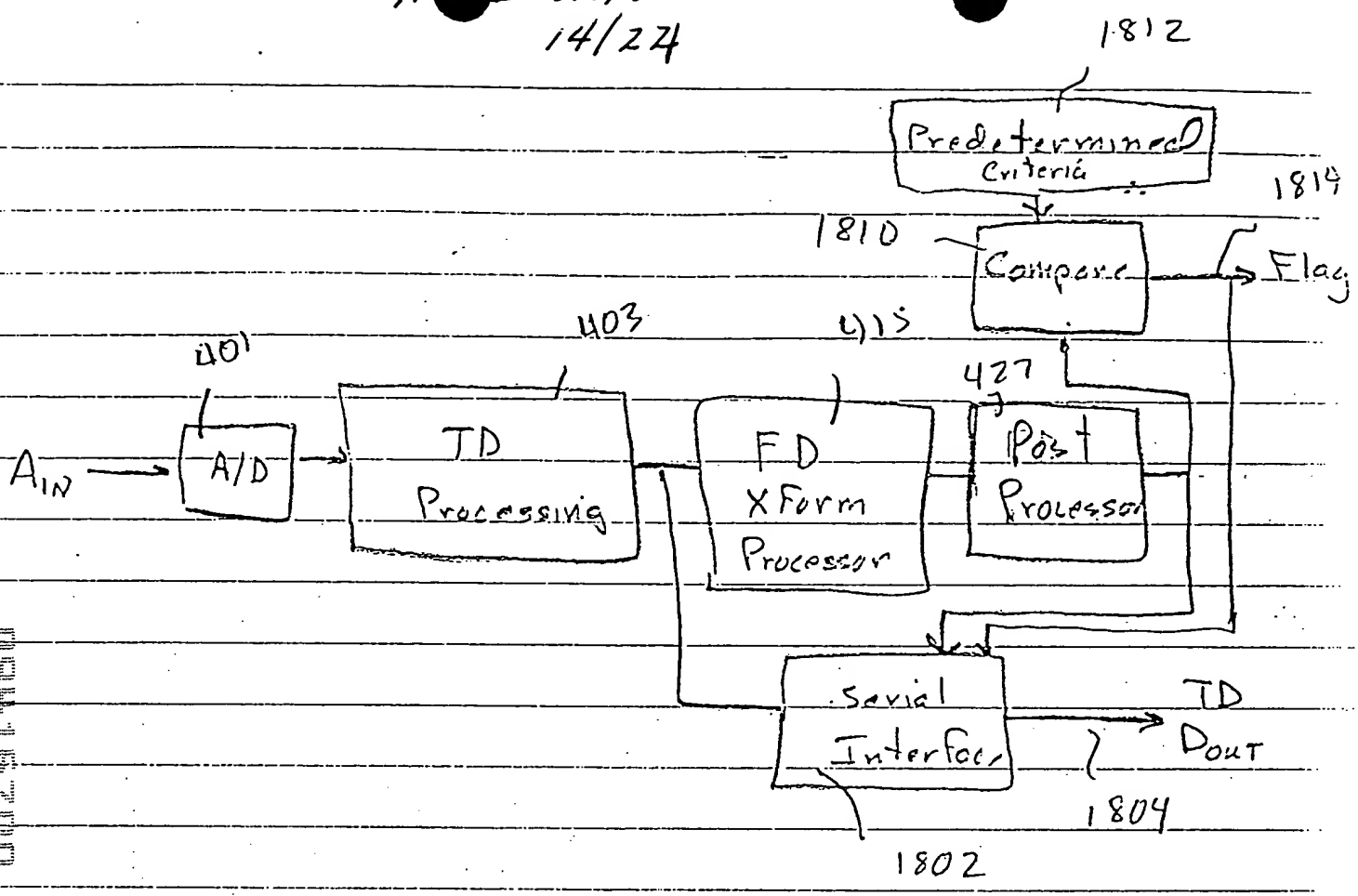

FIG 18

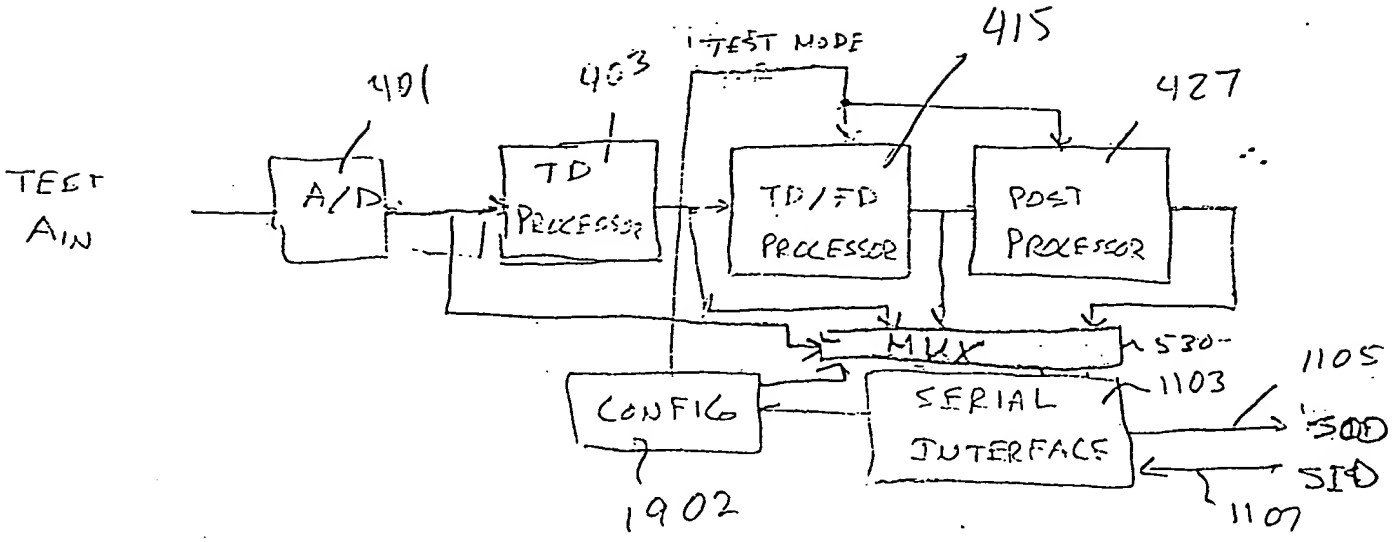

FIG 19a

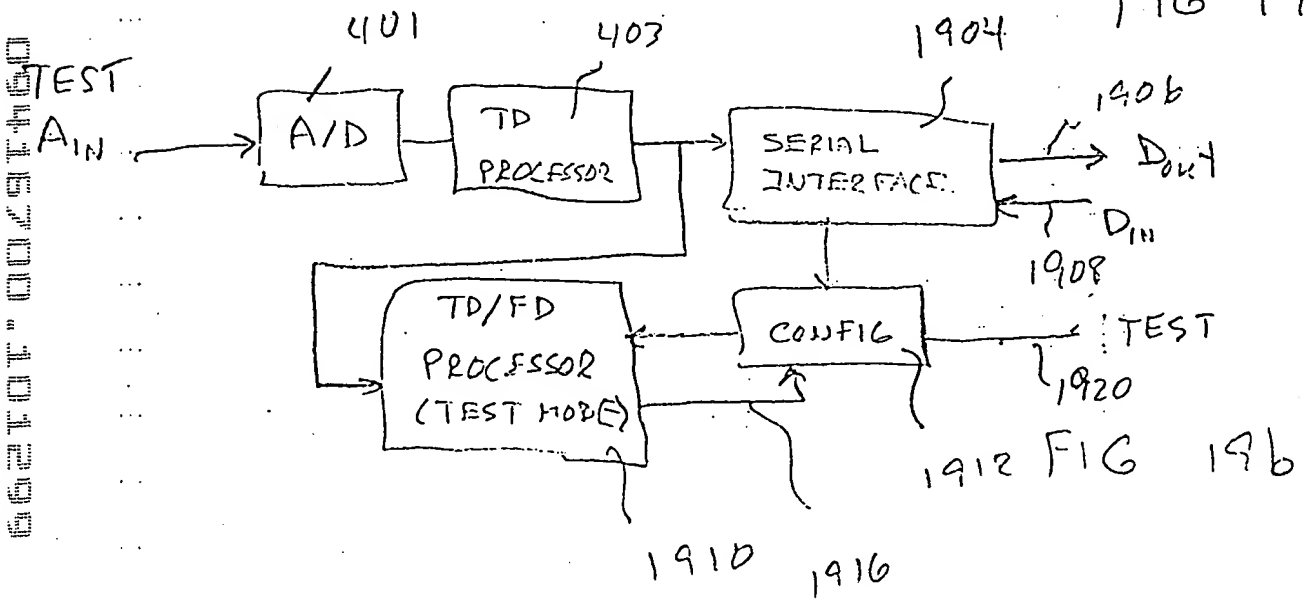

FIG 19b

Document: 1001142

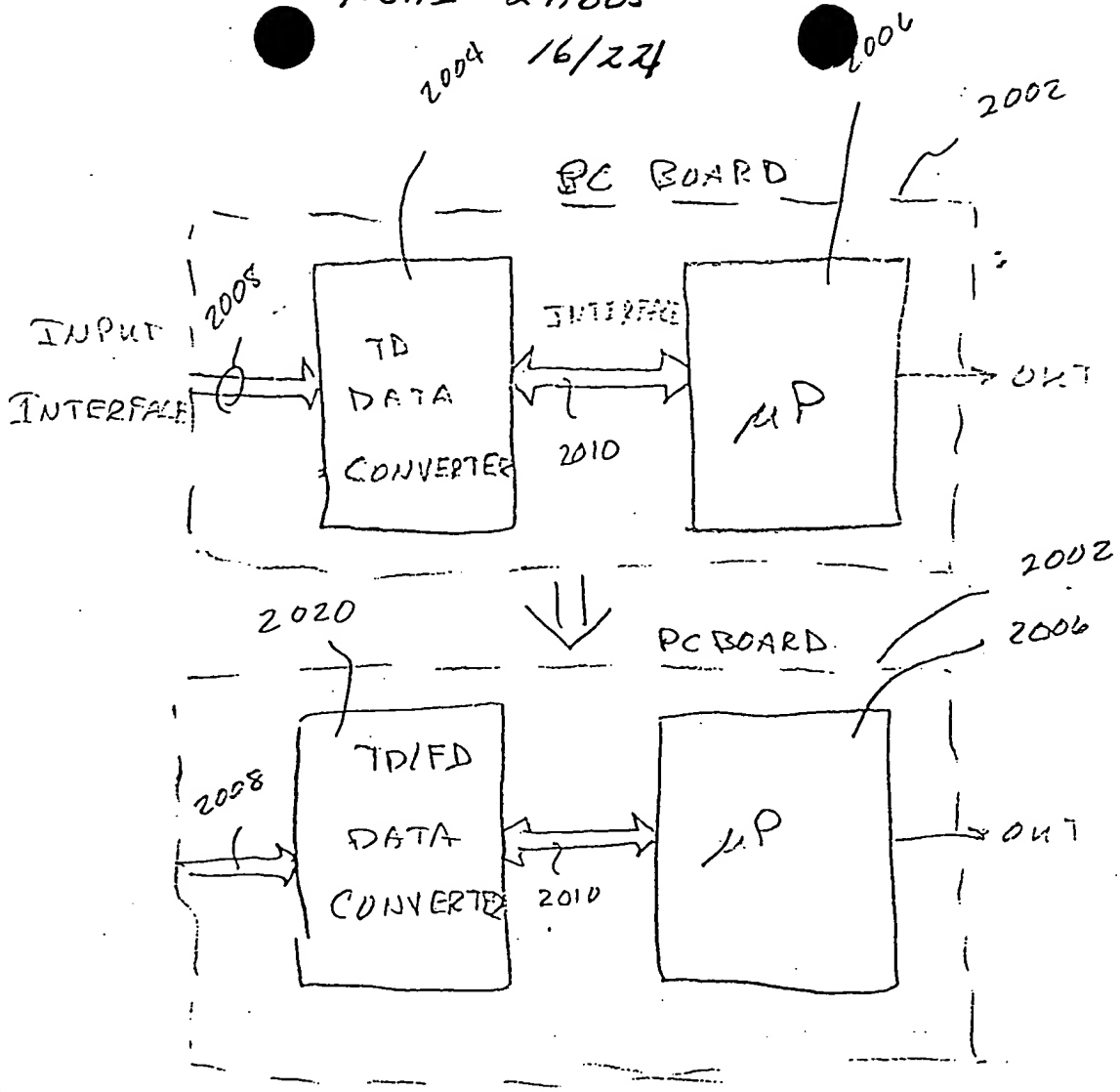

FIG 20

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HCAI-

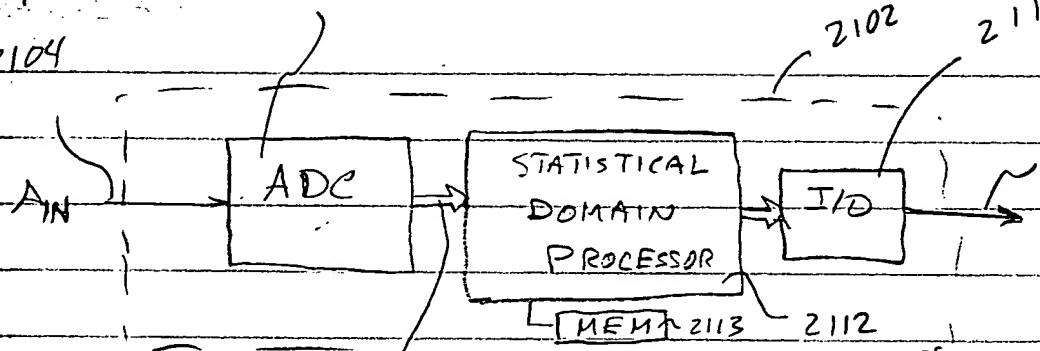

FIG 21

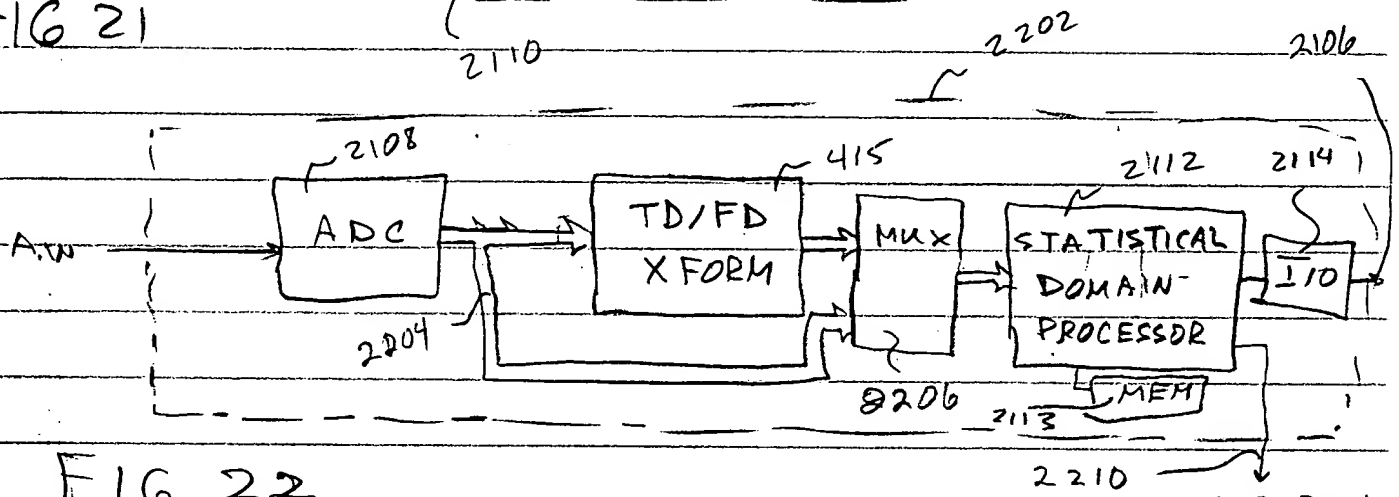

FIG 22

Confidential

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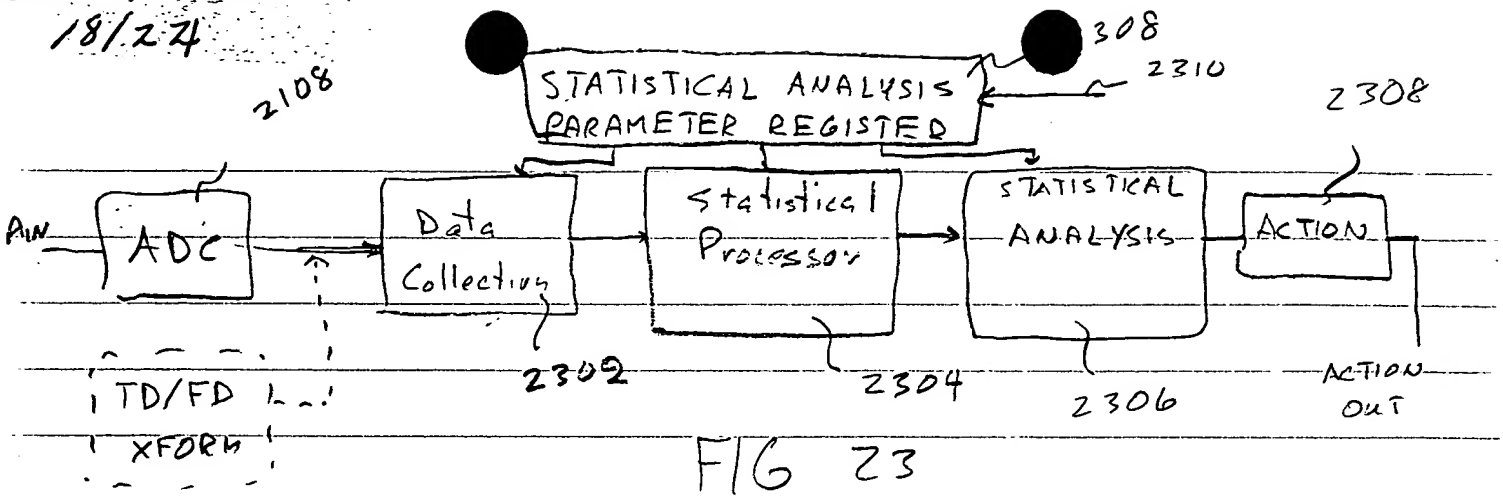

FIG 23

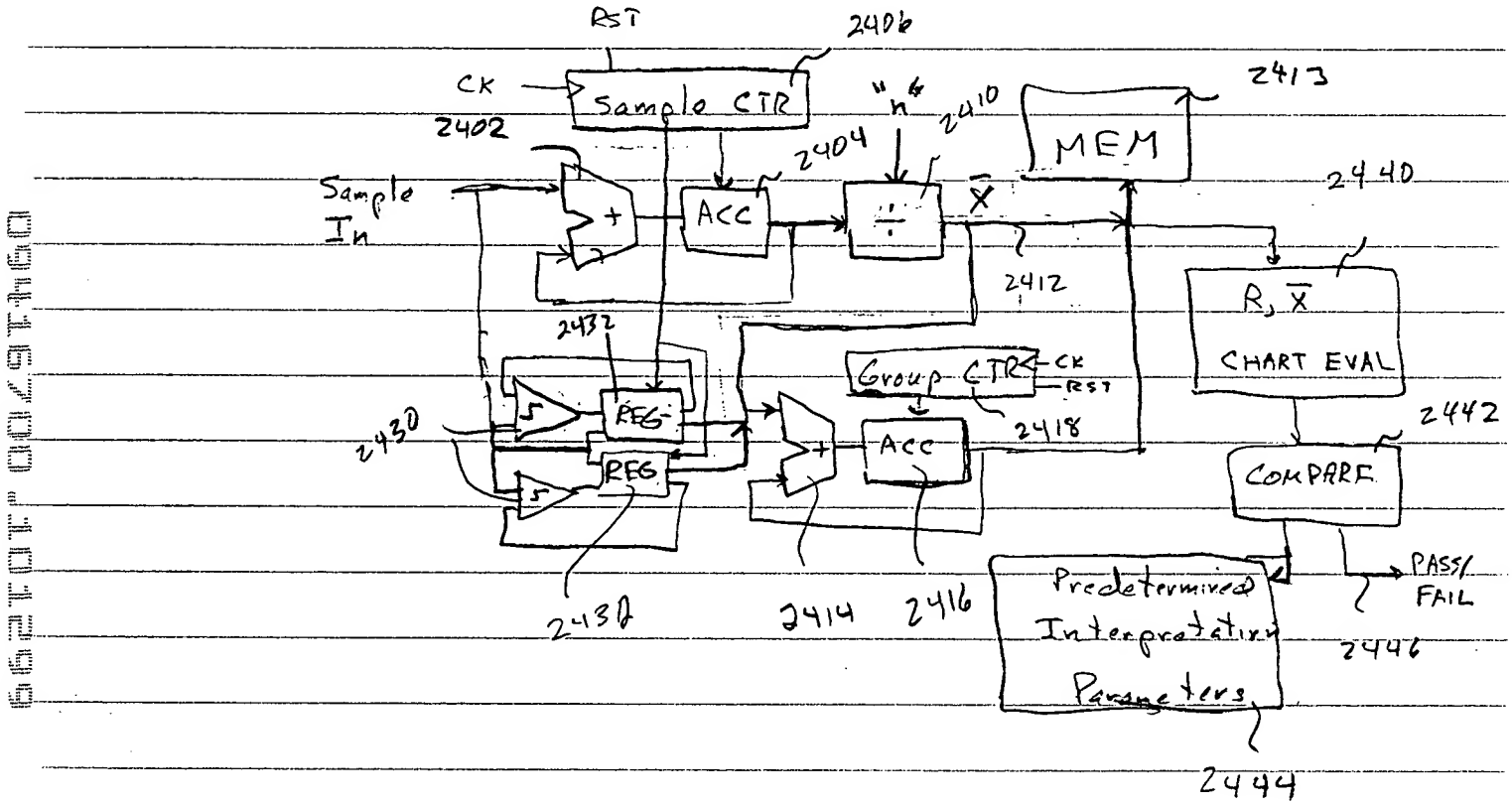

FIG 24

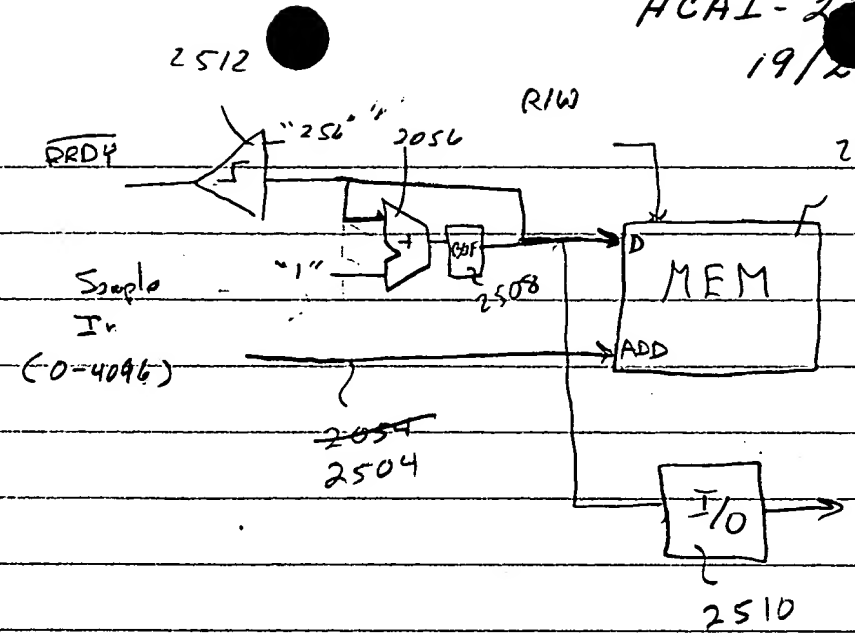

FIG 25

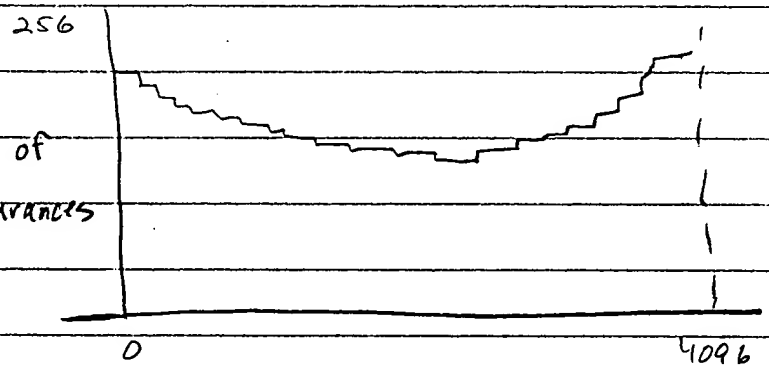

FIG 26

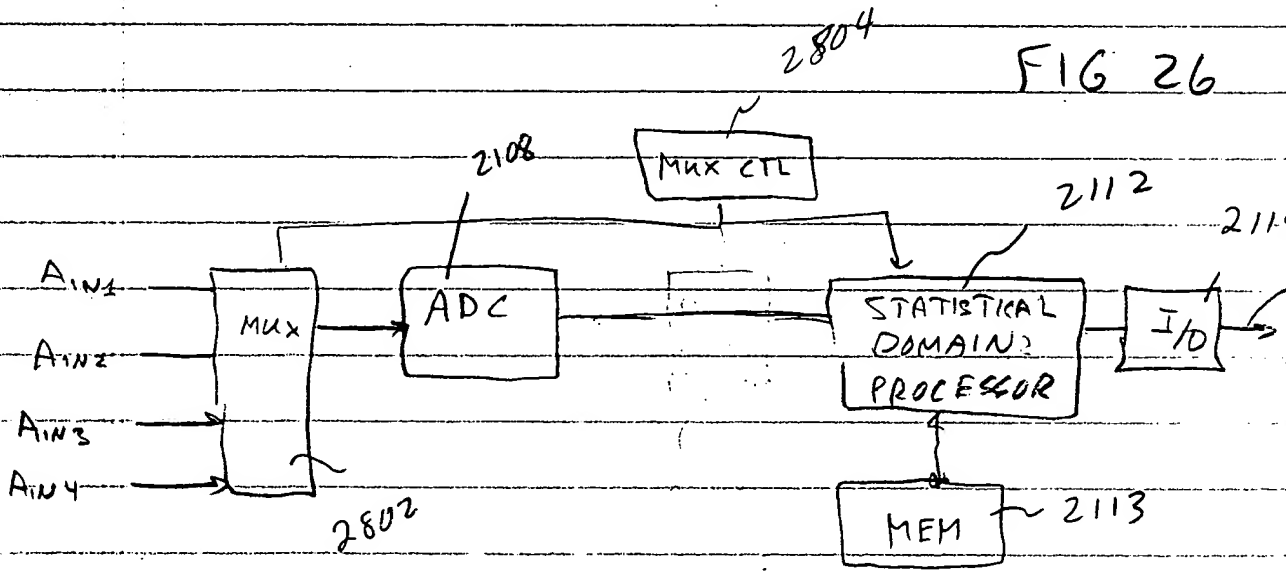

FIG 28

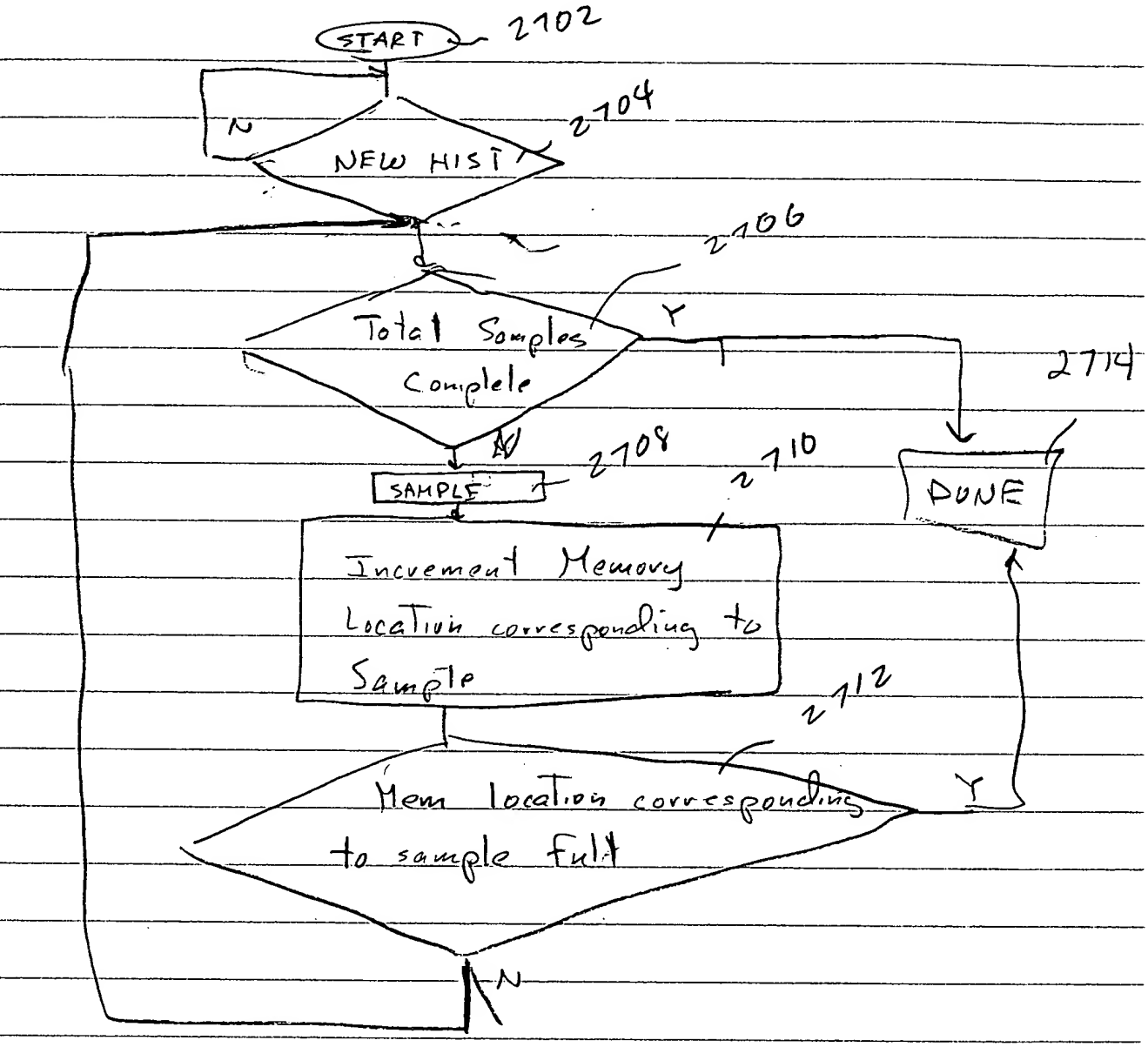
START
2702
N
NEW HIST
2704
2706
Total Samples Complete
Y
2714
N
SAMPLE
2708
2710
DONE
Increment Memory Location corresponding to Sample
2712
Mem location corresponding to sample full
Y
N

FIG 27

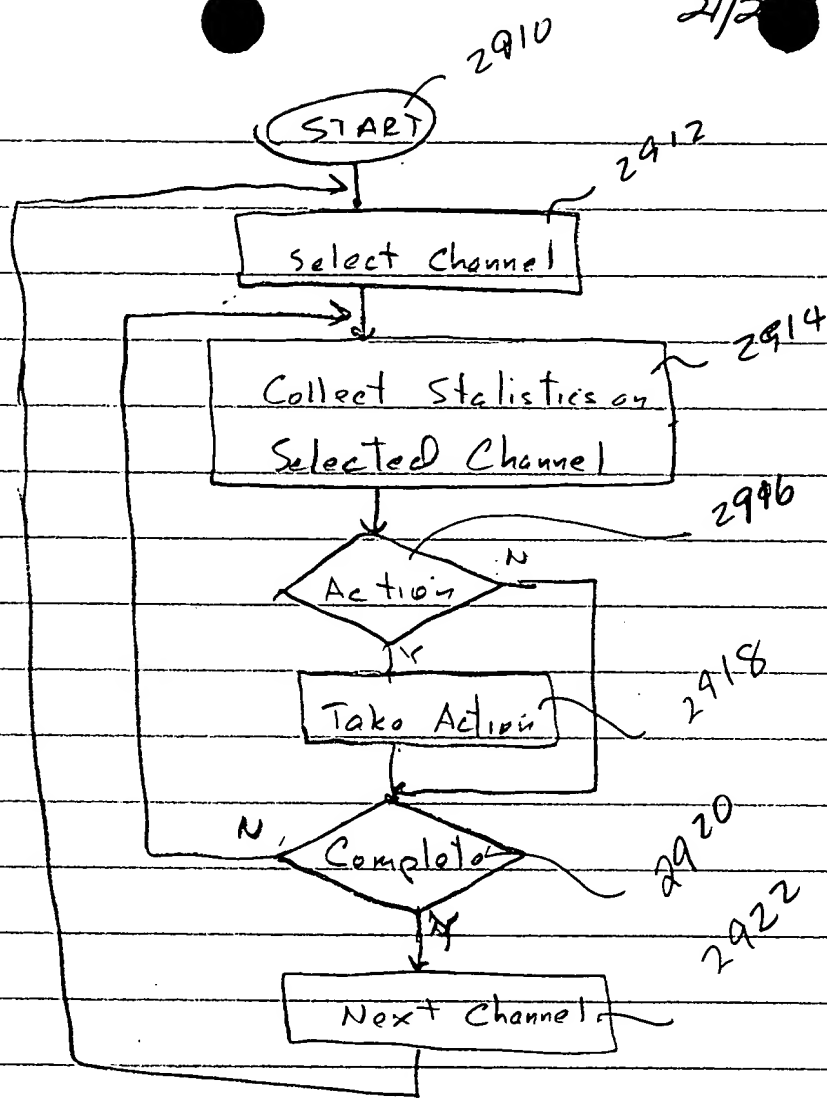

FIG 29

SUBSTITUTE SHEET (RULE 26)

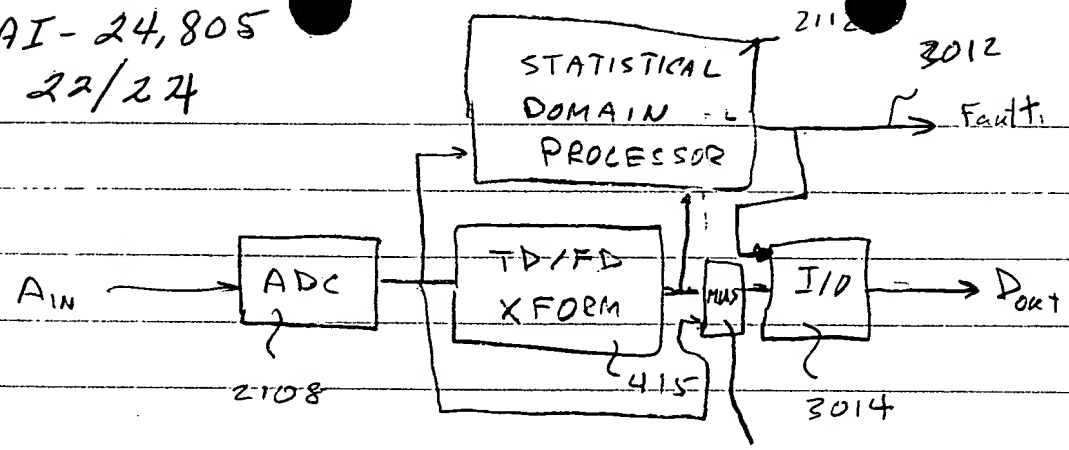
STATISTICAL DOMAIN PROCESSOR
2112
3012
Fault
ADC
TD/FD XFORM
MUX
I/O
A_{IN}
D_{OUT}
2108
415
3014
3010

FIG 30

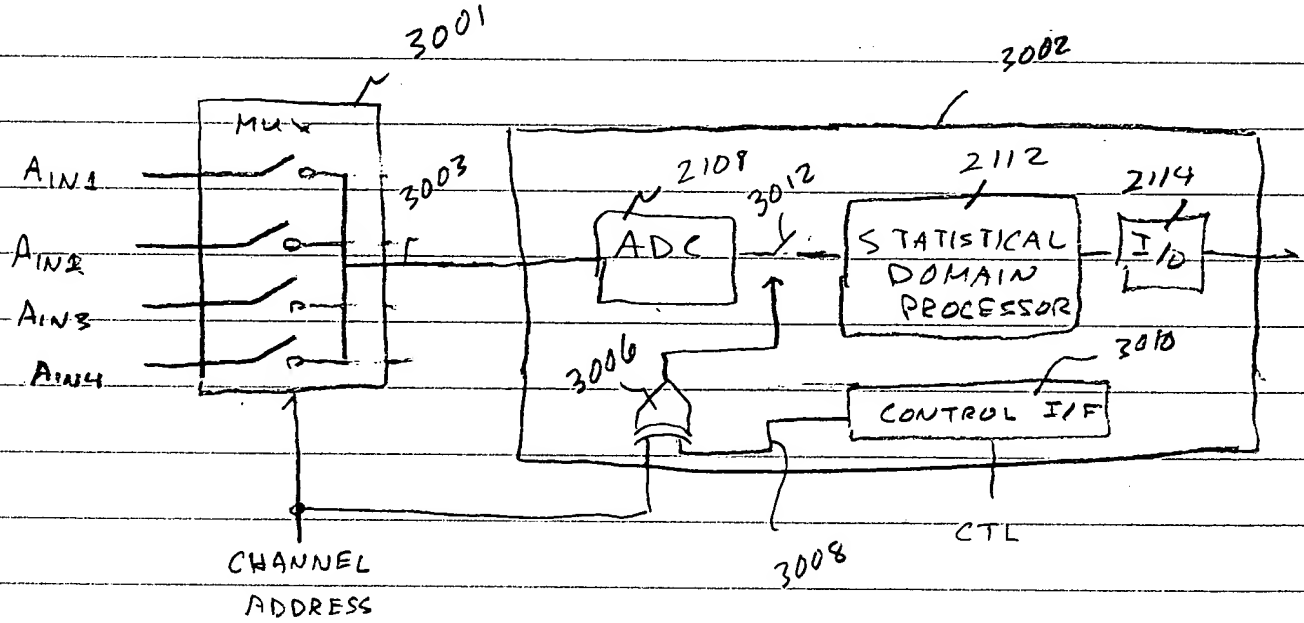
3001
3002
MUX
A_{IN1}
A_{IN2}
A_{IN3}
A_{IN4}
3003
2108
3012
2112
2114
ADC
STATISTICAL DOMAIN PROCESSOR
I/O
3006
3010
CONTROL I/F
CHANNEL ADDRESS
3008
CTL

FIG 31

6621OF"0029Fh60

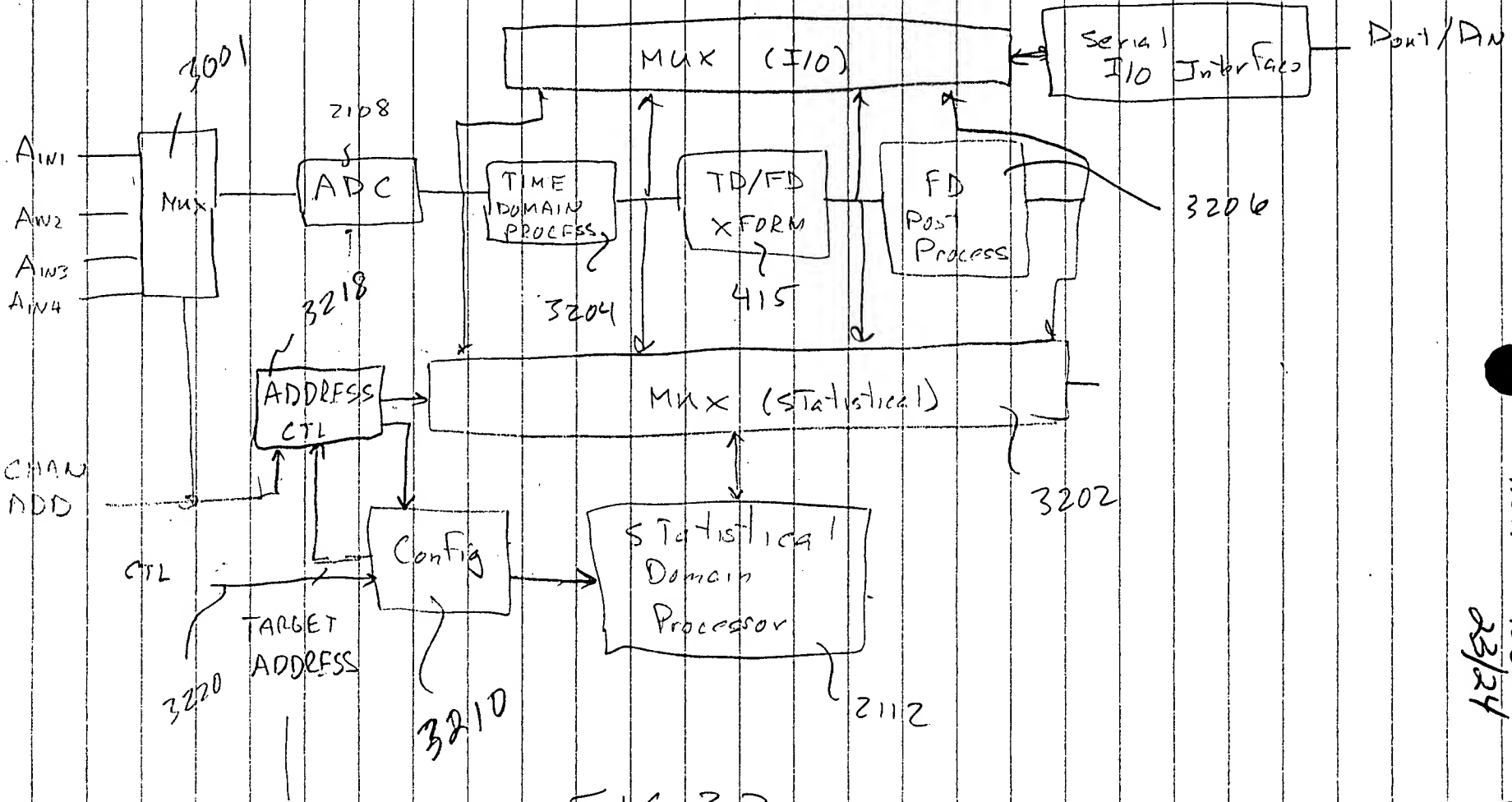

FIG 32

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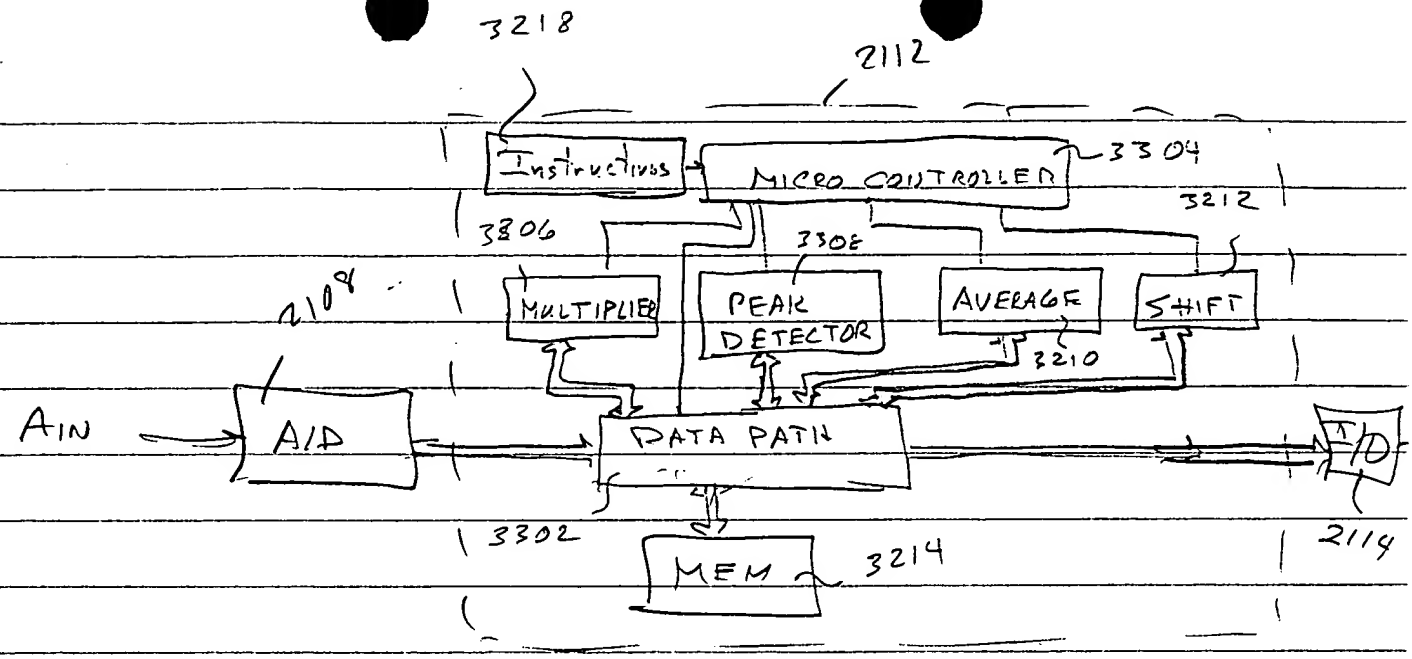

FIG 33

DOCUMENT-FOUND